



ocket No. 303.444US5  
WD # 454800

Micron Ref. No. 93-0305.04

**Clean Version of Pending Claims**

**METHOD OF DEPOSITING TUNGSTEN NITRIDE USING A SOURCE GAS COMPRISING SILICON**

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Serial No.: 10/004,714

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OCT 28 2002  
TECHNOLOGY CENTER 2800

*Claims 38-74, as of October 18, 2002 (date response to first office action filed).*

38. An integrated circuit capacitor comprising:  
a first electrode formed of polysilicon;  
a second electrode formed of chemically vapor deposited tungsten nitride formed using a gas comprising nitride, tungsten and silicon; and  
a dielectric layer located between the first and second electrodes.
39. The integrated circuit capacitor of claim 38 wherein the dielectric layer is comprised of tantalum oxide.
- B / 40. The integrated circuit capacitor of claim 38 wherein the capacitor is a memory cell.
41. (Amended) A capacitor, comprising:  
a first electrode;  
a second electrode; and  
a dielectric disposed between the first and the second electrode,  
wherein at least one of the first electrode and the second electrode includes a tungsten nitride layer, and the tungsten nitride layer includes silicon.
42. (Amended) The capacitor of claim 41, wherein both the first electrode and the second electrode includes a tungsten nitride layer, and the tungsten nitride layer includes silicon.
43. The capacitor of claim 41, wherein the capacitor is a non-planar capacitor.

44. The capacitor of claim 41, wherein the dielectric includes tantalum oxide.
45. The capacitor of claim 41, wherein the tungsten nitride prevents degradation of the dielectric.
46. (Amended) A capacitor, comprising:  
a first electrode;  
a dielectric disposed on the first electrode; and  
a second electrode formed on the dielectric as a layer of tungsten nitride, the layer of tungsten nitride including silicon.
- B1* 47. The capacitor of claim 46, wherein the capacitor is a non-planar capacitor.
48. The capacitor of claim 46, wherein the dielectric includes tantalum oxide.
49. (Amended) The capacitor of claim 46, wherein the layer of tungsten nitride is conformally deposited by chemical vapor deposition.
50. (Amended) The capacitor of claim 46, wherein the layer of tungsten nitride is exposed to silicon based materials, and wherein a boundary between the layer of tungsten nitride and the silicon based materials is characterized by a reduced encroachment of the tungsten nitride into the silicon based materials.
51. The capacitor of claim 46, wherein the first electrode is formed as a conformal polycrystalline silicon layer.

52. (Amended) A capacitor, comprising:  
a first electrode formed as a layer of tungsten nitride, the layer of tungsten nitride including silicon;  
a dielectric disposed on the first electrode; and  
a second electrode formed on the dielectric.

53. The capacitor of claim 52, wherein the capacitor is a non-planar capacitor.

54. The capacitor of claim 52, wherein the dielectric includes tantalum oxide.

B1 55. (Amended) The capacitor of claim 52, wherein the layer of tungsten nitride is conformally deposited by chemical vapor deposition.

56. (Amended) The capacitor of claim 52, wherein the layer of tungsten nitride is exposed to silicon based materials, and wherein a boundary between the layer of tungsten nitride and the silicon based materials is characterized by a reduced encroachment of the tungsten nitride into the silicon based materials.

57. The capacitor of claim 52, wherein the second electrode is formed as a polycrystalline silicon layer.

58. (Amended) A non-planar capacitor, comprising:  
a polycrystalline silicon film;  
a dielectric layer disposed on the polycrystalline film; and  
a film of tungsten nitride disposed on the dielectric layer, the film of tungsten nitride including silicon.

59. The non-planar capacitor of claim 58, wherein the polycrystalline silicon film is a conformal film formed over a substrate and over transistor devices on the substrate.

60. The non-planar capacitor of claim 58, wherein the dielectric layer includes tantalum oxide.

61. (Amended) The non-planar capacitor of claim 58, wherein the film of tungsten nitride is conformally deposited by chemical vapor deposition.

B' 62. (Amended) A non-planar capacitor, comprising:  
a conformal polycrystalline silicon film formed over a substrate and over transistor devices on the substrate;  
a dielectric layer formed on the conformal polycrystalline silicon film; and  
a film of tungsten nitride conformally deposited on the dielectric layer by chemical vapor deposition, the film of tungsten nitride including silicon.

63. (Amended) The non-planar capacitor of claim 62, wherein the film of tungsten nitride is formed by a chemical vapor deposition process that uses ammonia as a source of nitrogen and a gas selected from the group consisting of tungsten hexafluoride and tungsten carbonyl as a source of tungsten.

64. (Amended) The non-planar capacitor of claim 62, wherein the film of tungsten nitride is formed by a chemical vapor deposition process that uses a source gas mixture that includes:  
ammonia;  
a gas selected from the group consisting of tungsten hexafluoride and tungsten carbonyl;

and

a gas selected from the group consisting of silane, organic silane, and a compound that is a multiple order of silane.

65. The non-planar capacitor of claim 62, wherein the dielectric layer includes tantalum oxide.

66. (Amended) A non-planar capacitor, comprising:

a first electrode;

a dielectric layer formed on the first electrode; and

a film of tungsten nitride conformally deposited on the dielectric layer by chemical vapor deposition that uses gases, including:

ammonia;

a gas selected from the group consisting of tungsten hexafluoride and tungsten carbonyl; and

a gas selected from the group consisting of silane, organic silane, and a compound that is a multiple order of silane.

67. The non-planar capacitor of claim 66, wherein the first electrode includes a conformal polycrystalline silicon film formed over a substrate and over transistor devices on the substrate.

68. The non-planar capacitor of claim 66, wherein the gases used in the chemical vapor deposition process are a source gas mixture.

69. (Amended) An integrated circuit, comprising:

a substrate;

at least one transistor device formed on the substrate and arranged to leave a contact area

with the substrate;

a non-planar capacitor, including:

a first electrode;

a second electrode; and

a dielectric disposed between the first and the second electrode,

wherein at least one of the first electrode and the second electrode includes a tungsten nitride layer, and the tungsten nitride layer includes silicon.

*B1* 70. (Amended) The integrated circuit of claim 69, wherein both the first electrode and the second electrode includes a tungsten nitride layer, and the tungsten nitride layer includes silicon.

*Cont.* 71. (Amended) The integrated circuit of claim 69, wherein the first electrode includes a tungsten nitride layer, and the tungsten nitride layer includes silicon.

72. (Amended) The integrated circuit of claim 69, wherein the second electrode includes a tungsten nitride layer, and the tungsten nitride layer includes silicon.

73. The integrated circuit of claim 69, wherein the dielectric includes tantalum oxide.

74. The integrated circuit of claim 69, wherein the tungsten nitride prevents degradation of the dielectric.

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